Laboratory Report

**Course:** Coen 316 **Lab Section:** DL-X

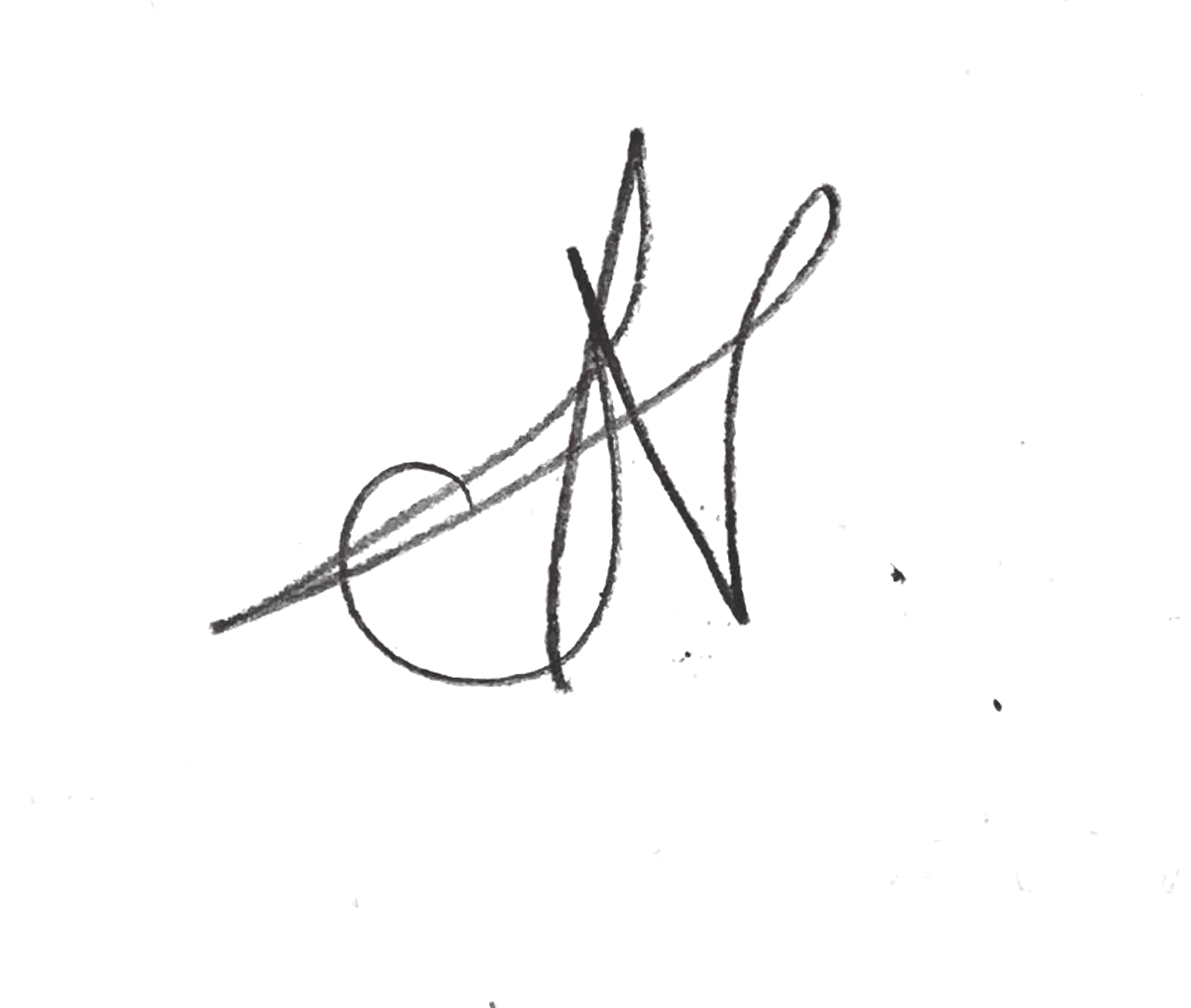
**Experiment No:** 4 **Date Performed:** 2023 – 11 – 09

**Report Due Date:** 2023 – 11 – 23

**Name:** Noah Louvet **ID:** 40086114

**I certify that this submission is my original work and meets the Faculty’s Expectations of Originality**

**Signature:**  **Date:** 2023 – 11-23



**Objectives**

In this lab, the main objective is to design a CPU. In order to design the CPU we first have to design the datapath as well as the missing units of the CPU. In the previous labs we have already designed the alu, regfile and next address unit. The remaining units to be designed and implemented are the instruction cache, the data cache, sign extender, pc and control unit. Once all units and datapath regulating how the units are connected to each other are designed, they are combined to implement the CPU. Additionally, is it adapted to be implemented on the Xilinx FPGA board.

**Introduction**

The MIPS processor implemented in these labs contains 20 instructions divided into three categories: R (register) , I (Immediate) and J (Jump) instructions.

A screen shot of a computer

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***Figure 1***: R-instruction table (source : lab manual)

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***Figure 2***: I-instruction table (source: lab manual)

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***Figure 3***: R-instruction table (source: lab manual)

**Results**

In this part I’ll be showing the results of the conducted lab with screenshots at every step as well as the different codes used to obtain the results.

A diagram of a computer program

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***Figure 4***: datapath

**ALU:**

**A screenshot of a computer program

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**A screenshot of a computer program

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**A screenshot of a computer code

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**I-CACHE**

****

**WAVEFORM**

**A document with numbers and lines

Description automatically generated**

**DO FILE**

add wave address

add wave instruction

force address 00000

run 2

force address 00001

run 2

force address 00010

run 2

force address 01011

run 2

force address 00110

run 2

force address 01111

run 2

**D-CACHE**

**A screenshot of a computer program

Description automatically generated**

**WAVEFORM**

**A screenshot of a computer

Description automatically generated**

**A black and white diagram

Description automatically generated with medium confidence**

**DO FILE**

add wave din

add wave reset

add wave clk

add wave data\_write

add wave address

add wave dout

#add wave all\_32\_registers

# show what happens in individual registers in the array

add wave all\_32\_registers(0)

add wave all\_32\_registers(1)

add wave all\_32\_registers(2)

add wave all\_32\_registers(3)

add wave all\_32\_registers(4)

add wave all\_32\_registers(5)

add wave all\_32\_registers(6)

add wave all\_32\_registers(7)

add wave all\_32\_registers(8)

add wave all\_32\_registers(9)

add wave all\_32\_registers(10)

add wave all\_32\_registers(11)

add wave all\_32\_registers(12)

add wave all\_32\_registers(13)

add wave all\_32\_registers(14)

add wave all\_32\_registers(15)

add wave all\_32\_registers(16)

add wave all\_32\_registers(17)

add wave all\_32\_registers(18)

add wave all\_32\_registers(19)

add wave all\_32\_registers(20)

add wave all\_32\_registers(21)

add wave all\_32\_registers(22)

add wave all\_32\_registers(23)

add wave all\_32\_registers(24)

add wave all\_32\_registers(25)

add wave all\_32\_registers(26)

add wave all\_32\_registers(27)

add wave all\_32\_registers(28)

add wave all\_32\_registers(29)

add wave all\_32\_registers(30)

add wave all\_32\_registers(31)

force din X"eb5cffc8"

force reset 0

force clk 0

force data\_write 0

force address 00000

run 2

force din X"0ad758a0"

force reset 0

force clk 1

force data\_write 1

force address 00000

run 2

force din X"a3986c6f"

force reset 0

force clk 0

force data\_write 0

force address 00000

run 2

force din X"0e5ef765"

force reset 0

force clk 1

force data\_write 1

force address 00001

run 2

force din X"203e7faa"

force reset 0

force clk 0

force data\_write 0

force address 00001

run 2

force din X"88104000"

force reset 0

force clk 1

force data\_write 1

force address 00010

run 2

force din X"72cc3d9e"

force reset 0

force clk 0

force data\_write 1

force address 00010

run 2

force din X"00004000"

force reset 0

force clk 1

force data\_write 1

force address 00011

run 2

force din X"4a5087f7"

force reset 0

force clk 0

force data\_write 0

force address 00011

run 2

force din X"0fbfc599"

force reset 0

force clk 1

force data\_write 1

force address 00100

run 2

force din X"00004000"

force reset 0

force clk 0

force data\_write 1

force address 00100

run 2

force din X"357439de"

force reset 0

force clk 1

force data\_write 1

force address 00101

run 2

force din X"00000028"

force reset 0

force clk 0

force data\_write 0

force address 00101

run 2

force din X"5ae3fd98"

force reset 0

force clk 1

force data\_write 1

force address 00110

run 2

force din X"00000002"

force reset 0

force clk 0

force data\_write 0

force address 00110

run 2

force din X"af1c6650"

force reset 0

force clk 1

force data\_write 1

force address 00111

run 2

force din X"00000001"

force reset 0

force clk 0

force data\_write 0

force address 00111

run 2

force din X"0000000F"

force reset 0

force clk 1

force data\_write 1

force address 01000

run 2

force din X"0000000B"

force reset 0

force clk 0

force data\_write 1

force address 01000

run 2

force din X"e76aed87"

force reset 0

force clk 1

force data\_write 1

force address 01001

run 2

force din X"d342ec23"

force reset 0

force clk 0

force data\_write 0

force address 01001

run 2

force din X"00000009"

force reset 0

force clk 1

force data\_write 1

force address 01010

run 2

force din X"c9b6d3e3"

force reset 0

force clk 0

force data\_write 1

force address 01010

run 2

force din X"0040000B"

force reset 0

force clk 1

force data\_write 1

force address 01011

run 2

force din X"0040001B"

force reset 0

force clk 0

force data\_write 1

force address 01011

run 2

force din X"f1acc020"

force reset 0

force clk 1

force data\_write 1

force address 01100

run 2

force din X"5a0cf281"

force reset 0

force clk 0

force data\_write 0

force address 01100

run 2

force din X"0040001A"

force reset 0

force clk 1

force data\_write 1

force address 01101

run 2

force din X"4cea1c7d"

force reset 0

force clk 0

force data\_write 0

force address 01101

run 2

force din X"0040003A"

force reset 0

force clk 1

force data\_write 1

force address 01110

run 2

force din X"0040003B"

force reset 0

force clk 0

force data\_write 0

force address 01110

run 2

force din X"a92341f4"

force reset 0

force clk 1

force data\_write 1

force address 01111

run 2

force din X"b6b97a7e"

force reset 0

force clk 0

force data\_write 1

force address 01111

run 2

force din X"0000023B"

force reset 0

force clk 1

force data\_write 1

force address 10000

run 2

force din X"081ff9cb"

force reset 0

force clk 0

force data\_write 1

force address 10000

run 2

force din X"0000027F"

force reset 0

force clk 1

force data\_write 1

force address 10001

run 2

force din X"5ed7a006"

force reset 0

force clk 0

force data\_write 0

force address 10001

run 2

force din X"0000027C"

force reset 0

force clk 1

force data\_write 1

force address 10010

run 2

force din X"82d5d9d9"

force reset 0

force clk 0

force data\_write 0

force address 10010

run 2

force din X"062a930d"

force reset 0

force clk 1

force data\_write 1

force address 10011

run 2

force din X"f9e14581"

force reset 0

force clk 0

force data\_write 0

force address 10011

run 2

force din X"000006FC"

force reset 0

force clk 1

force data\_write 1

force address 10100

run 2

force din X"6e20d89f"

force reset 0

force clk 0

force data\_write 0

force address 10100

run 2

force din X"000026FC"

force reset 0

force clk 1

force data\_write 1

force address 10101

run 2

force din X"271a81f9"

force reset 0

force clk 0

force data\_write 0

force address 10101

run 2

force din X"00006EFD"

force reset 0

force clk 1

force data\_write 1

force address 10110

run 2

force din X"aaa98e01"

force reset 0

force clk 0

force data\_write 0

force address 10110

run 2

force din X"00002EFD"

force reset 0

force clk 1

force data\_write 1

force address 10111

run 2

force din X"00012EFD"

force reset 0

force clk 0

force data\_write 0

force address 10111

run 2

force din X"f54a56a2"

force reset 0

force clk 1

force data\_write 1

force address 11000

run 2

force din X"00012EFF"

force reset 0

force clk 0

force data\_write 0

force address 11000

run 2

force din X"00012EFF"

force reset 0

force clk 1

force data\_write 1

force address 11001

run 2

force din X"00012EFD"

force reset 0

force clk 0

force data\_write 0

force address 11001

run 2

force din X"00012EFD"

force reset 0

force clk 1

force data\_write 1

force address 11010

run 2

force din X"00013EFD"

force reset 0

force clk 0

force data\_write 0

force address 11010

run 2

force din X"00013EFF"

force reset 0

force clk 1

force data\_write 1

force address 11011

run 2

force din X"00013EFF"

force reset 0

force clk 0

force data\_write 0

force address 11011

run 2

force din X"00013EFF"

force reset 0

force clk 1

force data\_write 1

force address 11100

run 2

force din X"00013EE7"

force reset 0

force clk 0

force data\_write 0

force address 11100

run 2

force din X"00013EE7"

force reset 0

force clk 1

force data\_write 1

force address 11101

run 2

force din X"b41c38e3"

force reset 0

force clk 0

force data\_write 0

force address 11101

run 2

force din X"00013FE7"

force reset 0

force clk 1

force data\_write 1

force address 11110

run 2

force din X"00017FE6"

force reset 0

force clk 0

force data\_write 0

force address 11110

run 2

force din X"00017FE6"

force reset 0

force clk 1

force data\_write 1

force address 11111

run 2

force din X"00017FEE"

force reset 0

force clk 0

force data\_write 0

force address 11111

run 2

force din X"00017FEE"

force reset 0

force clk 1

force data\_write 0

force address 11111

run 2

force din X"00000001"

force reset 0

force clk 0

force data\_write 0

force address 11111

run 2

force din X"00000001"

force reset 0

force clk 1

force data\_write 1

force address 10001

run 2

force din X"00000001"

force reset 0

force clk 0

force data\_write 0

force address 10001

run 2

force din X"00000003"

force reset 0

force clk 1

force data\_write 1

force address 10101

run 2

force din X"00000001"

force reset 0

force clk 0

force data\_write 0

force address 10101

run 2

force din X"00000083"

force reset 1

force clk 1

force data\_write 0

force address 10111

run 2

force din X"00000001"

force reset 0

force clk 0

force data\_write 1

force address 10111

run 2

force din X"00000001"

force reset 0

force clk 1

force data\_write 0

force address 10111

run 2

force din X"00000001"

force reset 0

force clk 0

force data\_write 1

force address 11111

run 2

force din X"00000001"

force reset 0

force clk 1

force data\_write 1

force address 11111

run 2

force din X"00000001"

force reset 1

force clk 0

force data\_write 1

force address 11111

run 2

force din X"00000001"

force reset 0

force clk 1

force data\_write 0

force address 11111

run 2

**PC REGISTER:**

**A screenshot of a computer program

Description automatically generated**

**SIGN EXTENSION:**

**A screenshot of a computer code

Description automatically generated**

**WAVEFORM:**

**A screenshot of a computer

Description automatically generated**

**DO FILE:**

add wave din

add wave func

add wave sign\_ext

force din X"0582"

force func 00

run 2

force din X"A019"

force func 01

run 2

force din X"E107"

force func 10

run 2

force din X"4FFF"

force func 11

run 2

**CONTROL UNIT:**

**Based on the below table**

**A table of numbers and symbols

Description automatically generated**

**A grid of black writing

Description automatically generated with medium confidence**

**A screen shot of a computer code

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A screen shot of a computer code

Description automatically generated

A screenshot of a computer code

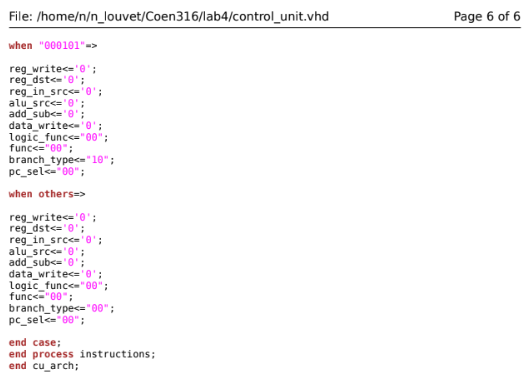
Description automatically generated

A screenshot of a computer program

Description automatically generated

A screen shot of a computer code

Description automatically generated



**CONTROL UNIT WAVEFORM**

A black and white chart

Description automatically generated

**CONTROL UNIT DO FILE:**

add wave op

add wave funct

add wave reg\_write

add wave reg\_dst

add wave reg\_in\_src

add wave alu\_src

add wave add\_sub

add wave data\_write

add wave logic\_func

add wave func

add wave add\_sub

add wave branch\_type

add wave pc\_sel

force op 000000

force funct 001000

run 2

force op 000000

force funct 101000

run 2

force op 000000

force funct 100000

run 2

force op 000000

force funct 101011

run 2

force op 000000

force funct 110100

run 2

force op 000000

force funct 100110

run 2

force op 000000

force funct 111101

run 2

force op 000000

force funct 110010

run 2

force op 000000

force funct 100011

run 2

force op 000000

force funct 111111

run 2

force op 001111

force funct 100101

run 2

force op 001000

force funct 100100

run 2

force op 001010

force funct 111111

run 2

force op 001100

force funct 100100

run 2

force op 001101

force funct 100100

run 2

force op 001110

force funct 100100

run 2

force op 100011

force funct 100100

run 2

force op 101011

force funct 111111

run 2

force op 000010

force funct 100100

run 2

force op 000001

force funct 100100

run 2

force op 000100

force funct 111111

run 2

force op 000101

force funct 100100

run 2

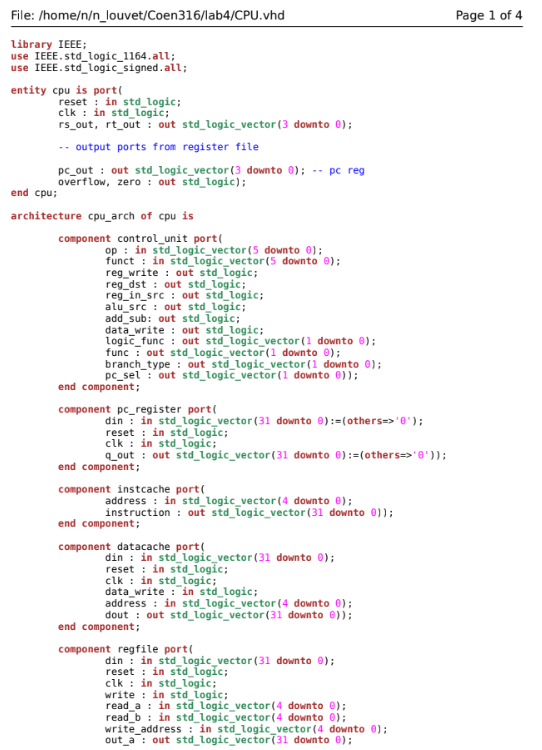
force op 111111

force funct 100100

run 2

**CPU:**

Combining all the components together we obtain the CPU



A screen shot of a computer code

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A screenshot of a computer program

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A screenshot of a computer code

Description automatically generated

**WAVEFORM**

A diagram of a number

Description automatically generated with medium confidence

Vivado logs can be found in the appendix section.

**Conclusion**

In conclusion, this lab delved into the complex mechanisms of building a CPU. We started by building the fundamental building blocks. The lab's core involved the remaining units that hadn’t already been designed in the previous labs. Through meticulous analysis of our building blocks and individual testing we were able to integrate all the different units together to build the CPU. As a result, all deliverables were provided, and the lab was a success.

**Appendix**

**Vivado Synthesis**

\*\*\* Running vivado

with args -log cpu.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source cpu.tcl

\*\*\*\*\*\* Vivado v2018.2 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

\*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source cpu.tcl -notrace

Command: synth\_design -top cpu -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 18715

---------------------------------------------------------------------------------

Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1401.582 ; gain = 85.805 ; free physical = 10996 ; free virtual = 22859

---------------------------------------------------------------------------------

INFO: [Synth 8-638] synthesizing module 'cpu' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/CPU.vhd:13]

INFO: [Synth 8-3491] module 'control\_unit' declared at '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/control\_unit.vhd:5' bound to instance 'controller' of component 'control\_unit' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/CPU.vhd:125]

INFO: [Synth 8-638] synthesizing module 'control\_unit' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/control\_unit.vhd:19]

INFO: [Synth 8-256] done synthesizing module 'control\_unit' (1#1) [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/control\_unit.vhd:19]

INFO: [Synth 8-3491] module 'pc\_register' declared at '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/pc\_register.vhd:6' bound to instance 'pc\_reg' of component 'pc\_register' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/CPU.vhd:139]

INFO: [Synth 8-638] synthesizing module 'pc\_register' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/pc\_register.vhd:13]

INFO: [Synth 8-256] done synthesizing module 'pc\_register' (2#1) [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/pc\_register.vhd:13]

INFO: [Synth 8-3491] module 'instcache' declared at '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/instcache.vhd:5' bound to instance 'instruction\_cache' of component 'instcache' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/CPU.vhd:145]

INFO: [Synth 8-638] synthesizing module 'instcache' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/instcache.vhd:10]

INFO: [Synth 8-256] done synthesizing module 'instcache' (3#1) [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/instcache.vhd:10]

INFO: [Synth 8-3491] module 'datacache' declared at '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/datacache.vhd:6' bound to instance 'dcache' of component 'datacache' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/CPU.vhd:149]

INFO: [Synth 8-638] synthesizing module 'datacache' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/datacache.vhd:15]

INFO: [Synth 8-256] done synthesizing module 'datacache' (4#1) [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/datacache.vhd:15]

INFO: [Synth 8-3491] module 'regfile' declared at '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/regfile.vhd:6' bound to instance 'register\_file' of component 'regfile' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/CPU.vhd:157]

INFO: [Synth 8-638] synthesizing module 'regfile' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/regfile.vhd:18]

WARNING: [Synth 8-614] signal 'registers' is read in the process but is not in the sensitivity list [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/regfile.vhd:42]

INFO: [Synth 8-256] done synthesizing module 'regfile' (5#1) [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/regfile.vhd:18]

INFO: [Synth 8-3491] module 'alu' declared at '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/alu.vhd:5' bound to instance 'cpu\_alu' of component 'alu' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/CPU.vhd:168]

INFO: [Synth 8-638] synthesizing module 'alu' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/alu.vhd:15]

INFO: [Synth 8-256] done synthesizing module 'alu' (6#1) [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/alu.vhd:15]

INFO: [Synth 8-3491] module 'signextend' declared at '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/signextend.vhd:6' bound to instance 'sign\_extender' of component 'signextend' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/CPU.vhd:178]

INFO: [Synth 8-638] synthesizing module 'signextend' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/signextend.vhd:12]

INFO: [Synth 8-256] done synthesizing module 'signextend' (7#1) [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/signextend.vhd:12]

INFO: [Synth 8-3491] module 'next\_address' declared at '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/next\_address.vhd:6' bound to instance 'next\_addr' of component 'next\_address' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/CPU.vhd:185]

INFO: [Synth 8-638] synthesizing module 'next\_address' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/next\_address.vhd:15]

WARNING: [Synth 8-614] signal 'branch\_offset' is read in the process but is not in the sensitivity list [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/next\_address.vhd:36]

INFO: [Synth 8-256] done synthesizing module 'next\_address' (8#1) [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/next\_address.vhd:15]

INFO: [Synth 8-256] done synthesizing module 'cpu' (9#1) [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/CPU.vhd:13]

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Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1447.223 ; gain = 131.445 ; free physical = 11002 ; free virtual = 22866

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1447.223 ; gain = 131.445 ; free physical = 11005 ; free virtual = 22868

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1447.223 ; gain = 131.445 ; free physical = 11005 ; free virtual = 22868

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INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/constrs\_1/imports/lab4/lab4.xdc]

Finished Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/constrs\_1/imports/lab4/lab4.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/constrs\_1/imports/lab4/lab4.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/cpu\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/cpu\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1843.977 ; gain = 0.000 ; free physical = 10758 ; free virtual = 22620

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Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10838 ; free virtual = 22700

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10838 ; free virtual = 22700

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10839 ; free virtual = 22701

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INFO: [Synth 8-5546] ROM "reg\_write" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5587] ROM size for "alu\_src" is below threshold of ROM address width. It will be mapped to LUTs

INFO: [Synth 8-5587] ROM size for "add\_sub" is below threshold of ROM address width. It will be mapped to LUTs

INFO: [Synth 8-5546] ROM "data\_write" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "logic\_func" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5587] ROM size for "func" is below threshold of ROM address width. It will be mapped to LUTs

INFO: [Synth 8-5546] ROM "branch\_type" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "pc\_sel" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "instruction" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[0]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[1]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[2]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[3]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[4]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[5]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[6]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[7]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[8]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[9]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[10]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[11]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[12]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[13]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[14]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[15]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[16]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[17]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[18]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[19]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[20]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[21]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[22]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[23]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[24]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[25]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[26]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[27]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[28]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[29]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[30]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[31]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[0]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[1]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[2]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[3]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[4]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[5]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[6]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[7]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[8]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[9]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[10]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[11]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[12]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[13]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[14]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[15]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[16]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[17]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[18]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[19]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[20]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[21]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[22]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[23]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[24]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[25]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[26]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[27]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[28]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[29]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[30]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "registers\_reg[31]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/alu.vhd:33]

WARNING: [Synth 8-327] inferring latch for variable 'out\_func\_reg' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/alu.vhd:71]

WARNING: [Synth 8-327] inferring latch for variable 'next\_pc\_reg' [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/sources\_1/imports/lab4/next\_address.vhd:66]

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10829 ; free virtual = 22692

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

3 Input 32 Bit Adders := 1

2 Input 32 Bit Adders := 2

+---XORs :

2 Input 32 Bit XORs := 1

+---Registers :

32 Bit Registers := 65

+---Muxes :

2 Input 32 Bit Muxes := 7

4 Input 32 Bit Muxes := 5

2 Input 30 Bit Muxes := 1

4 Input 30 Bit Muxes := 1

2 Input 5 Bit Muxes := 1

9 Input 2 Bit Muxes := 3

14 Input 2 Bit Muxes := 4

3 Input 2 Bit Muxes := 1

9 Input 1 Bit Muxes := 2

14 Input 1 Bit Muxes := 6

2 Input 1 Bit Muxes := 65

4 Input 1 Bit Muxes := 2

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Finished RTL Component Statistics

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Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module cpu

Detailed RTL Component Info :

+---Muxes :

2 Input 32 Bit Muxes := 2

2 Input 5 Bit Muxes := 1

Module control\_unit

Detailed RTL Component Info :

+---Muxes :

9 Input 2 Bit Muxes := 3

14 Input 2 Bit Muxes := 4

3 Input 2 Bit Muxes := 1

9 Input 1 Bit Muxes := 2

14 Input 1 Bit Muxes := 6

Module pc\_register

Detailed RTL Component Info :

+---Registers :

32 Bit Registers := 1

Module instcache

Detailed RTL Component Info :

+---Muxes :

2 Input 30 Bit Muxes := 1

4 Input 30 Bit Muxes := 1

Module datacache

Detailed RTL Component Info :

+---Registers :

32 Bit Registers := 32

+---Muxes :

2 Input 1 Bit Muxes := 32

Module regfile

Detailed RTL Component Info :

+---Registers :

32 Bit Registers := 32

+---Muxes :

2 Input 1 Bit Muxes := 32

Module alu

Detailed RTL Component Info :

+---Adders :

3 Input 32 Bit Adders := 1

+---XORs :

2 Input 32 Bit XORs := 1

+---Muxes :

2 Input 32 Bit Muxes := 1

4 Input 32 Bit Muxes := 2

2 Input 1 Bit Muxes := 1

4 Input 1 Bit Muxes := 1

Module signextend

Detailed RTL Component Info :

+---Muxes :

4 Input 32 Bit Muxes := 1

Module next\_address

Detailed RTL Component Info :

+---Adders :

2 Input 32 Bit Adders := 2

+---Muxes :

2 Input 32 Bit Muxes := 4

4 Input 32 Bit Muxes := 2

4 Input 1 Bit Muxes := 1

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[31][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[30][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[30][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[29][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[29][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[28][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[28][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[27][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[27][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[26][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[26][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[25][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[25][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[24][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[24][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[23][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[23][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[22][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[22][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[21][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[21][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[20][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[20][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[19][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[19][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[18][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[18][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[17][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[17][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[16][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[16][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[15][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[15][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[14][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[14][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[13][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[13][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[12][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[12][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[11][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[11][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[10][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[10][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[9][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[9][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[8][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[8][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[7][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[7][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[6][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[6][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[5][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[5][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[4][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[4][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[3][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[3][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[2][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[2][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[1][4]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[1][4]' (FDCE) to 'dcache/all\_32\_registers\_reg[0][4]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][4] )

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[31][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[30][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[30][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[29][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[29][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[28][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[28][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[27][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[27][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[26][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[26][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[25][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[25][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[24][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[24][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[23][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[23][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[22][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[22][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[21][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[21][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[20][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[20][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[19][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[19][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[18][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[18][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[17][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[17][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[16][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[16][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[15][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[15][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[14][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[14][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[13][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[13][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[12][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[12][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[11][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[11][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[10][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[10][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[9][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[9][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[8][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[8][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[7][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[7][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[6][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[6][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[5][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[5][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[4][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[4][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[3][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[3][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[2][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[2][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[1][5]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[1][5]' (FDCE) to 'dcache/all\_32\_registers\_reg[0][5]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][5] )

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[31][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[30][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[30][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[29][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[29][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[28][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[28][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[27][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[27][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[26][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[26][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[25][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[25][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[24][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[24][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[23][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[23][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[22][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[22][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[21][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[21][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[20][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[20][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[19][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[19][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[18][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[18][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[17][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[17][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[16][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[16][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[15][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[15][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[14][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[14][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[13][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[13][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[12][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[12][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[11][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[11][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[10][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[10][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[9][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[9][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[8][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[8][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[7][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[7][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[6][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[6][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[5][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[5][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[4][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[4][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[3][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[3][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[2][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[2][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[1][6]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[1][6]' (FDCE) to 'dcache/all\_32\_registers\_reg[0][6]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][6] )

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[31][7]' (FDCE) to 'dcache/all\_32\_registers\_reg[30][7]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[30][7]' (FDCE) to 'dcache/all\_32\_registers\_reg[29][7]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[29][7]' (FDCE) to 'dcache/all\_32\_registers\_reg[28][7]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[28][7]' (FDCE) to 'dcache/all\_32\_registers\_reg[27][7]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[27][7]' (FDCE) to 'dcache/all\_32\_registers\_reg[26][7]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[26][7]' (FDCE) to 'dcache/all\_32\_registers\_reg[25][7]'

INFO: [Synth 8-3886] merging instance 'dcache/all\_32\_registers\_reg[25][7]' (FDCE) to 'dcache/all\_32\_registers\_reg[24][7]'

INFO: [Common 17-14] Message 'Synth 8-3886' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set\_msg\_config to change the current settings.

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][7] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][8] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][9] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][10] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][11] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][12] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][13] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][14] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][15] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][16] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][17] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][18] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][19] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][20] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][21] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][22] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][23] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][24] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][25] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][26] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][27] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][28] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][29] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][30] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][31] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][0] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][1] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][2] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\dcache/all\_32\_registers\_reg[0][3] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][4] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][5] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][6] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][7] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][8] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][9] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][10] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][11] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][12] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][13] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][14] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][15] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][16] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][17] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][18] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][19] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][20] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][21] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][22] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][23] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][24] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][25] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][26] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][27] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][28] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][29] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][30] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][31] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][0] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][1] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][2] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[4][3] )

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][4]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][5]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][6]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][7]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][8]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][9]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][10]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][11]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][12]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][13]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][14]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][15]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][16]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][17]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][18]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][19]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][20]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][21]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][22]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][23]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][24]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][25]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][26]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][27]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][28]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][29]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][30]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][31]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][0]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][1]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][2]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (dcache/all\_32\_registers\_reg[0][3]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][4]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][5]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][6]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][7]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][8]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][9]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][10]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][11]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][12]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][13]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][14]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][15]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][16]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][17]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][18]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][19]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][20]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][21]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][22]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][23]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][24]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][25]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][26]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][27]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][28]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][29]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][30]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][31]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][0]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][1]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][2]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (register\_file/registers\_reg[4][3]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[31]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[30]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[29]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[28]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[27]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[26]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[25]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[24]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[23]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[22]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[21]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[20]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[19]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[18]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[17]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[16]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[15]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[14]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[13]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[12]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[11]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[10]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[9]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[8]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[7]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[6]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[5]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[4]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[3]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[2]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[1]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (cpu\_alu/out\_func\_reg[0]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (next\_addr/next\_pc\_reg[31]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (next\_addr/next\_pc\_reg[30]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (next\_addr/next\_pc\_reg[29]) is unused and will be removed from module cpu.

WARNING: [Synth 8-3332] Sequential element (next\_addr/next\_pc\_reg[28]) is unused and will be removed from module cpu.

INFO: [Common 17-14] Message 'Synth 8-3332' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set\_msg\_config to change the current settings.

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][4] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][5] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][6] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][7] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][8] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][9] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][10] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][11] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][12] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][13] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][14] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][15] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][16] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][17] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][18] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][19] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][20] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][21] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][22] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][23] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][24] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][25] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][26] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][27] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][28] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][29] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][30] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][31] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][0] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][1] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][2] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\register\_file/registers\_reg[0][3] )

---------------------------------------------------------------------------------

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:12 ; elapsed = 00:00:40 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10808 ; free virtual = 22673

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start Applying XDC Timing Constraints

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---------------------------------------------------------------------------------

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:16 ; elapsed = 00:00:50 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10682 ; free virtual = 22548

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---------------------------------------------------------------------------------

Start Timing Optimization

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---------------------------------------------------------------------------------

Finished Timing Optimization : Time (s): cpu = 00:00:16 ; elapsed = 00:00:50 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10682 ; free virtual = 22548

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:16 ; elapsed = 00:00:50 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10680 ; free virtual = 22546

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start IO Insertion

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---------------------------------------------------------------------------------

Start Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Finished Flattening Before IO Insertion

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished IO Insertion : Time (s): cpu = 00:00:17 ; elapsed = 00:00:51 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10680 ; free virtual = 22546

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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---------------------------------------------------------------------------------

Finished Renaming Generated Instances : Time (s): cpu = 00:00:17 ; elapsed = 00:00:51 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10680 ; free virtual = 22546

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:17 ; elapsed = 00:00:51 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10680 ; free virtual = 22546

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---------------------------------------------------------------------------------

Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:17 ; elapsed = 00:00:51 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10680 ; free virtual = 22546

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---------------------------------------------------------------------------------

Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:17 ; elapsed = 00:00:51 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10680 ; free virtual = 22546

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:17 ; elapsed = 00:00:51 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10680 ; free virtual = 22546

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Start Writing Synthesis Report

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Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |BUFG | 1|

|2 |CARRY4 | 9|

|3 |LUT1 | 1|

|4 |LUT3 | 30|

|5 |LUT4 | 8|

|6 |LUT5 | 7|

|7 |LUT6 | 72|

|8 |FDCE | 69|

|9 |IBUF | 2|

|10 |OBUF | 14|

+------+-------+------+

Report Instance Areas:

+------+----------------+-------------+------+

| |Instance |Module |Cells |

+------+----------------+-------------+------+

|1 |top | | 213|

|2 | cpu\_alu |alu | 14|

|3 | next\_addr |next\_address | 1|

|4 | pc\_reg |pc\_register | 83|

|5 | register\_file |regfile | 98|

+------+----------------+-------------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:17 ; elapsed = 00:00:51 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10680 ; free virtual = 22546

---------------------------------------------------------------------------------

Synthesis finished with 0 errors, 0 critical warnings and 221 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:10 ; elapsed = 00:00:20 . Memory (MB): peak = 1843.977 ; gain = 131.445 ; free physical = 10734 ; free virtual = 22600

Synthesis Optimization Complete : Time (s): cpu = 00:00:17 ; elapsed = 00:00:51 . Memory (MB): peak = 1843.977 ; gain = 528.199 ; free physical = 10744 ; free virtual = 22610

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 11 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

310 Infos, 104 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:18 ; elapsed = 00:00:52 . Memory (MB): peak = 1843.980 ; gain = 540.852 ; free physical = 10731 ; free virtual = 22597

WARNING: [Constraints 18-5210] No constraint will be written out.

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.runs/synth\_1/cpu.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file cpu\_utilization\_synth.rpt -pb cpu\_utilization\_synth.pb

report\_utilization: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.10 . Memory (MB): peak = 1868.000 ; gain = 0.000 ; free physical = 10732 ; free virtual = 22598

INFO: [Common 17-206] Exiting Vivado at Wed Nov 22 15:57:59 2023...

**Vivado Implementation**

\*\*\* Running vivado

with args -log cpu.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source cpu.tcl -notrace

\*\*\*\*\*\* Vivado v2018.2 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source cpu.tcl -notrace

Command: link\_design -top cpu -part xc7a100tcsg324-1

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Netlist 29-17] Analyzing 11 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.2

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/constrs\_1/imports/lab4/lab4.xdc]

Finished Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.srcs/constrs\_1/imports/lab4/lab4.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

link\_design completed successfully

link\_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:31 . Memory (MB): peak = 1652.375 ; gain = 344.242 ; free physical = 10916 ; free virtual = 22778

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1744.402 ; gain = 92.027 ; free physical = 10908 ; free virtual = 22770

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: 19fce4a1d

Time (s): cpu = 00:00:09 ; elapsed = 00:00:36 . Memory (MB): peak = 2197.898 ; gain = 453.496 ; free physical = 10426 ; free virtual = 22288

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 19fce4a1d

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2197.898 ; gain = 0.000 ; free physical = 10499 ; free virtual = 22361

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 19fce4a1d

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2197.898 ; gain = 0.000 ; free physical = 10499 ; free virtual = 22361

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 14e3be725

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2197.898 ; gain = 0.000 ; free physical = 10499 ; free virtual = 22361

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 14e3be725

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2197.898 ; gain = 0.000 ; free physical = 10499 ; free virtual = 22361

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: ee30b549

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2197.898 ; gain = 0.000 ; free physical = 10499 ; free virtual = 22361

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: ee30b549

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2197.898 ; gain = 0.000 ; free physical = 10499 ; free virtual = 22361

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2197.898 ; gain = 0.000 ; free physical = 10499 ; free virtual = 22361

Ending Logic Optimization Task | Checksum: ee30b549

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2197.898 ; gain = 0.000 ; free physical = 10499 ; free virtual = 22361

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: ee30b549

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2197.902 ; gain = 0.004 ; free physical = 10499 ; free virtual = 22361

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: ee30b549

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2197.902 ; gain = 0.000 ; free physical = 10499 ; free virtual = 22361

INFO: [Common 17-83] Releasing license: Implementation

23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:11 ; elapsed = 00:00:38 . Memory (MB): peak = 2197.902 ; gain = 545.527 ; free physical = 10499 ; free virtual = 22361

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2229.918 ; gain = 0.004 ; free physical = 10497 ; free virtual = 22360

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.runs/impl\_1/cpu\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file cpu\_drc\_opted.rpt -pb cpu\_drc\_opted.pb -rpx cpu\_drc\_opted.rpx

Command: report\_drc -file cpu\_drc\_opted.rpt -pb cpu\_drc\_opted.pb -rpx cpu\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.runs/impl\_1/cpu\_drc\_opted.rpt.

report\_drc completed successfully

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2309.957 ; gain = 0.000 ; free physical = 10465 ; free virtual = 22327

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: b9aefd8d

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2309.957 ; gain = 0.000 ; free physical = 10465 ; free virtual = 22327

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2309.957 ; gain = 0.000 ; free physical = 10465 ; free virtual = 22327

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

WARNING: [Place 30-574] Poor placement for routing between an IO pin and BUFG. This is normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.

clk\_IBUF\_inst (IBUF.O) is locked to IOB\_X0Y82

clk\_IBUF\_BUFG\_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL\_X0Y0

Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: a5a3366e

Time (s): cpu = 00:00:00.97 ; elapsed = 00:00:00.45 . Memory (MB): peak = 2309.957 ; gain = 0.000 ; free physical = 10464 ; free virtual = 22327

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 1012a31bf

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.47 . Memory (MB): peak = 2309.957 ; gain = 0.000 ; free physical = 10464 ; free virtual = 22327

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 1012a31bf

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.47 . Memory (MB): peak = 2309.957 ; gain = 0.000 ; free physical = 10464 ; free virtual = 22327

Phase 1 Placer Initialization | Checksum: 1012a31bf

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.47 . Memory (MB): peak = 2309.957 ; gain = 0.000 ; free physical = 10464 ; free virtual = 22327

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: 1012a31bf

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.49 . Memory (MB): peak = 2309.957 ; gain = 0.000 ; free physical = 10463 ; free virtual = 22325

WARNING: [Place 46-29] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 173ac10e7

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.85 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10441 ; free virtual = 22303

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 173ac10e7

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.85 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10441 ; free virtual = 22303

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 193920705

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.87 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10442 ; free virtual = 22304

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 19d872667

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.88 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10442 ; free virtual = 22304

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 19d872667

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.88 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10442 ; free virtual = 22304

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 1426c54d0

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.99 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10438 ; free virtual = 22301

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 1426c54d0

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10438 ; free virtual = 22301

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 1426c54d0

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10438 ; free virtual = 22301

Phase 3 Detail Placement | Checksum: 1426c54d0

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10438 ; free virtual = 22301

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 1426c54d0

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10438 ; free virtual = 22301

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 1426c54d0

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10440 ; free virtual = 22302

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 1426c54d0

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10440 ; free virtual = 22302

Phase 4.4 Final Placement Cleanup

Phase 4.4 Final Placement Cleanup | Checksum: 14db0055d

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10440 ; free virtual = 22302

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 14db0055d

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10440 ; free virtual = 22302

Ending Placer Task | Checksum: 1439dfdc7

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2363.977 ; gain = 54.020 ; free physical = 10456 ; free virtual = 22318

INFO: [Common 17-83] Releasing license: Implementation

41 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2363.977 ; gain = 0.000 ; free physical = 10454 ; free virtual = 22318

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.runs/impl\_1/cpu\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file cpu\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2363.977 ; gain = 0.000 ; free physical = 10449 ; free virtual = 22312

INFO: [runtcl-4] Executing : report\_utilization -file cpu\_utilization\_placed.rpt -pb cpu\_utilization\_placed.pb

report\_utilization: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2363.977 ; gain = 0.000 ; free physical = 10456 ; free virtual = 22319

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file cpu\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2363.977 ; gain = 0.000 ; free physical = 10456 ; free virtual = 22319

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 8 threads

WARNING: [DRC PLCK-12] Clock Placer Checks: Poor placement for routing between an IO pin and BUFG.

Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.

This is normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.

clk\_IBUF\_inst (IBUF.O) is locked to IOB\_X0Y82

clk\_IBUF\_BUFG\_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL\_X0Y0

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 8 CPUs

Checksum: PlaceDB: b14ac033 ConstDB: 0 ShapeSum: 92533d94 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 1464b6042

Time (s): cpu = 00:00:15 ; elapsed = 00:00:13 . Memory (MB): peak = 2404.977 ; gain = 41.000 ; free physical = 10320 ; free virtual = 22183

Post Restoration Checksum: NetGraph: 9ac67bb6 NumContArr: ab84e48c Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 1464b6042

Time (s): cpu = 00:00:15 ; elapsed = 00:00:13 . Memory (MB): peak = 2409.965 ; gain = 45.988 ; free physical = 10289 ; free virtual = 22152

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 1464b6042

Time (s): cpu = 00:00:15 ; elapsed = 00:00:13 . Memory (MB): peak = 2409.965 ; gain = 45.988 ; free physical = 10289 ; free virtual = 22152

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: 11ad074c2

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2419.230 ; gain = 55.254 ; free physical = 10280 ; free virtual = 22143

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 89dfe45e

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2419.230 ; gain = 55.254 ; free physical = 10281 ; free virtual = 22144

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 41

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: 14c02fd26

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2419.230 ; gain = 55.254 ; free physical = 10284 ; free virtual = 22147

Phase 4 Rip-up And Reroute | Checksum: 14c02fd26

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2419.230 ; gain = 55.254 ; free physical = 10284 ; free virtual = 22147

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: 14c02fd26

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2419.230 ; gain = 55.254 ; free physical = 10284 ; free virtual = 22147

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: 14c02fd26

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2419.230 ; gain = 55.254 ; free physical = 10284 ; free virtual = 22147

Phase 6 Post Hold Fix | Checksum: 14c02fd26

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2419.230 ; gain = 55.254 ; free physical = 10284 ; free virtual = 22147

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.0256779 %

Global Horizontal Routing Utilization = 0.0200341 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 27.027%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 13.2353%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 23.5294%, No Congested Regions.

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Reporting congestion hotspots

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Direction: North

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 14c02fd26

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2419.230 ; gain = 55.254 ; free physical = 10284 ; free virtual = 22147

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 14c02fd26

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2422.230 ; gain = 58.254 ; free physical = 10283 ; free virtual = 22145

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 12b8b5b36

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2422.230 ; gain = 58.254 ; free physical = 10283 ; free virtual = 22145

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2422.230 ; gain = 58.254 ; free physical = 10317 ; free virtual = 22180

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

54 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:18 ; elapsed = 00:00:16 . Memory (MB): peak = 2422.234 ; gain = 58.258 ; free physical = 10317 ; free virtual = 22180

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.17 ; elapsed = 00:00:00.14 . Memory (MB): peak = 2422.234 ; gain = 0.000 ; free physical = 10316 ; free virtual = 22180

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.runs/impl\_1/cpu\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file cpu\_drc\_routed.rpt -pb cpu\_drc\_routed.pb -rpx cpu\_drc\_routed.rpx

Command: report\_drc -file cpu\_drc\_routed.rpt -pb cpu\_drc\_routed.pb -rpx cpu\_drc\_routed.rpx

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.runs/impl\_1/cpu\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file cpu\_methodology\_drc\_routed.rpt -pb cpu\_methodology\_drc\_routed.pb -rpx cpu\_methodology\_drc\_routed.rpx

Command: report\_methodology -file cpu\_methodology\_drc\_routed.rpt -pb cpu\_methodology\_drc\_routed.pb -rpx cpu\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 8 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /nfs/home/n/n\_louvet/Coen316/lab4/cpu vivado/cpu/cpu.runs/impl\_1/cpu\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file cpu\_power\_routed.rpt -pb cpu\_power\_summary\_routed.pb -rpx cpu\_power\_routed.rpx

Command: report\_power -file cpu\_power\_routed.rpt -pb cpu\_power\_summary\_routed.pb -rpx cpu\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

66 Infos, 4 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file cpu\_route\_status.rpt -pb cpu\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file cpu\_timing\_summary\_routed.rpt -pb cpu\_timing\_summary\_routed.pb -rpx cpu\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file cpu\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file cpu\_clock\_utilization\_routed.rpt

INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file cpu\_bus\_skew\_routed.rpt -pb cpu\_bus\_skew\_routed.pb -rpx cpu\_bus\_skew\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

INFO: [Common 17-206] Exiting Vivado at Wed Nov 22 16:03:38 2023...

\*\*\* Running vivado

with args -log cpu.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source cpu.tcl -notrace

\*\*\*\*\*\* Vivado v2018.2 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source cpu.tcl -notrace

Command: open\_checkpoint cpu\_routed.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1277.109 ; gain = 0.000 ; free physical = 11222 ; free virtual = 23085

INFO: [Netlist 29-17] Analyzing 11 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.2

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2089.059 ; gain = 0.004 ; free physical = 10470 ; free virtual = 22334

Restored from archive | CPU: 0.210000 secs | Memory: 1.132195 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2089.059 ; gain = 0.004 ; free physical = 10470 ; free virtual = 22334

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

open\_checkpoint: Time (s): cpu = 00:00:17 ; elapsed = 00:01:08 . Memory (MB): peak = 2089.059 ; gain = 811.953 ; free physical = 10470 ; free virtual = 22333

Command: write\_bitstream -force cpu.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 8 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./cpu.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Common 17-83] Releasing license: Implementation

21 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:08 ; elapsed = 00:00:12 . Memory (MB): peak = 2561.898 ; gain = 472.840 ; free physical = 10394 ; free virtual = 22265

INFO: [Common 17-206] Exiting Vivado at Wed Nov 22 16:06:43 2023...